Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. – 80. (cancelled.)

81. (currently amended) A method of reading a MONOS memory cell, wherein the MONOS memory cell comprises:

a word gate on the surface of a semiconductor substrate;

sidewall control gates on sidewalls of said word gate, separated from said word gates by an insulating layer;

nitride regions within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions;

a polysilicon word line overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and

bit line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates.;

wherein one of said nitride regions is a selected nitride region, and the other of said nitride regions is an unselected nitride region, and wherein said bit line diffusion

near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion,

wherein a read operation of said cell is performed by:

over-riding said unselected nitride region;

providing a voltage on said word gate having a sum of the word gate threshold voltage, an overdrive voltage, and the voltage on said source diffusion;

providing a voltage on said control gate adjacent to said selected nitride region sufficient to allow for reading of the selected nitride region; and

reading said cell by measuring the voltage level on said bit diffusion.

82. (original) A method of programming a MONOS memory cell, wherein said MONOS memory cell comprises:

a word gate on the surface of a semiconductor substrate;

sidewall control gates on sidewalls of said word gate, separated from said word gates by an insulating layer;

nitride regions within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions;

a polysilicon word line overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and

bit line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates;

wherein one of said control gates is a selected control gate and its underlying nitride region is a selected nitride region, and the other of said control gates is an unselected control gate and its underlying nitride region is an unselected nitride region, and wherein said bit line diffusion near said selected nitride region is a bit diffusion, and said bit line diffusion near said unselected nitride region is a source diffusion,

wherein said method of programming the cell comprises the steps of:

providing a high voltage on said unselected control gate to over-ride said unselected nitride region; and

varying a voltage on said selected control gate.

83. (currently amended) A method of erasing a MONOS memory cell, wherein said MONOS memory cell comprises:

a word gate on the surface of a semiconductor substrate;

sidewall control gates on sidewalls of said word gate, separated from said word gates by an insulating layer;

nitride regions within an ONO layer underlying said sidewall control gates wherein electron memory storage is performed within said nitride regions;

a polysilicon word line overlying and connecting said word gate with word gates in other said memory cells and overlying said sidewall control gates, separated from said sidewall control gates by an insulating layer; and

bit line diffusions within said semiconductor substrate adjacent to each of said sidewall control gates;

wherein said method of erasing a block of said nitride regions comprises the steps of:

providing a ~~positive~~ first voltage to said bit line diffusions; and

providing a ~~negative~~ second voltage opposite to said first voltage to said control gate over said bit line diffusions.

84. – 86. (cancelled.)

87. (new) The method according to Claim 81 wherein said memory cell is one of many cells in a MONOS memory array, and further comprising applying a control gate voltage of 0 volts to all cells beside the cell desired to be read.

88. (new) The method according to Claim 81 wherein said memory cell is one of many cells in a MONOS memory array, and further comprising applying a control gate voltage of –0.7 volts to all cells beside the cell desired to be read in order to stop leakage.

89. (new) The method according to Claim 81 wherein a voltage level on said bit diffusions represents one of multiple threshold levels of said cell.

90. (new) The method according to Claim 82 further comprising:

raising a control gate voltage of said selected nitride region;

providing a fixed voltage on said bit diffusion;

providing a voltage on said word gate which is greater than said word gate threshold voltage; and

lowering a voltage of said source diffusion such that current flows from said source diffusion to said bit diffusion wherein ballistic injection of electrons occurs from a channel region to said selected nitride region when current flows.

91. (new) The method according to Claim 82 wherein multiple thresholds can be programmed by varying a voltage on said bit line diffusions.

92. (new) The method according to Claim 82 wherein said memory cell is one of many cells in a MONOS memory array, and further comprising disabling nitride regions in adjacent cells sharing a word line by applying a control gate voltage of 0 volts to said adjacent cells.

93. (new) The method according to Claim 82 wherein said memory cell is one of many cells in a flash memory array that share a word line, and further comprising simultaneously programming several of said cells with different threshold levels by varying a voltage either of said sidewall control gates or said bit line diffusions.

94. (new) The method according to Claim 83 wherein said first voltage is a positive voltage and wherein said second voltage is a negative voltage.

95. (new) The method according to Claim 83 said first voltage is a negative voltage wherein said negative voltage is also applied to said semiconductor substrate and wherein said second voltage is a positive voltage.